ADE-207-040

HD63487
Memory Interface and Video Attribute Controller (MIVAC)

HITACHI

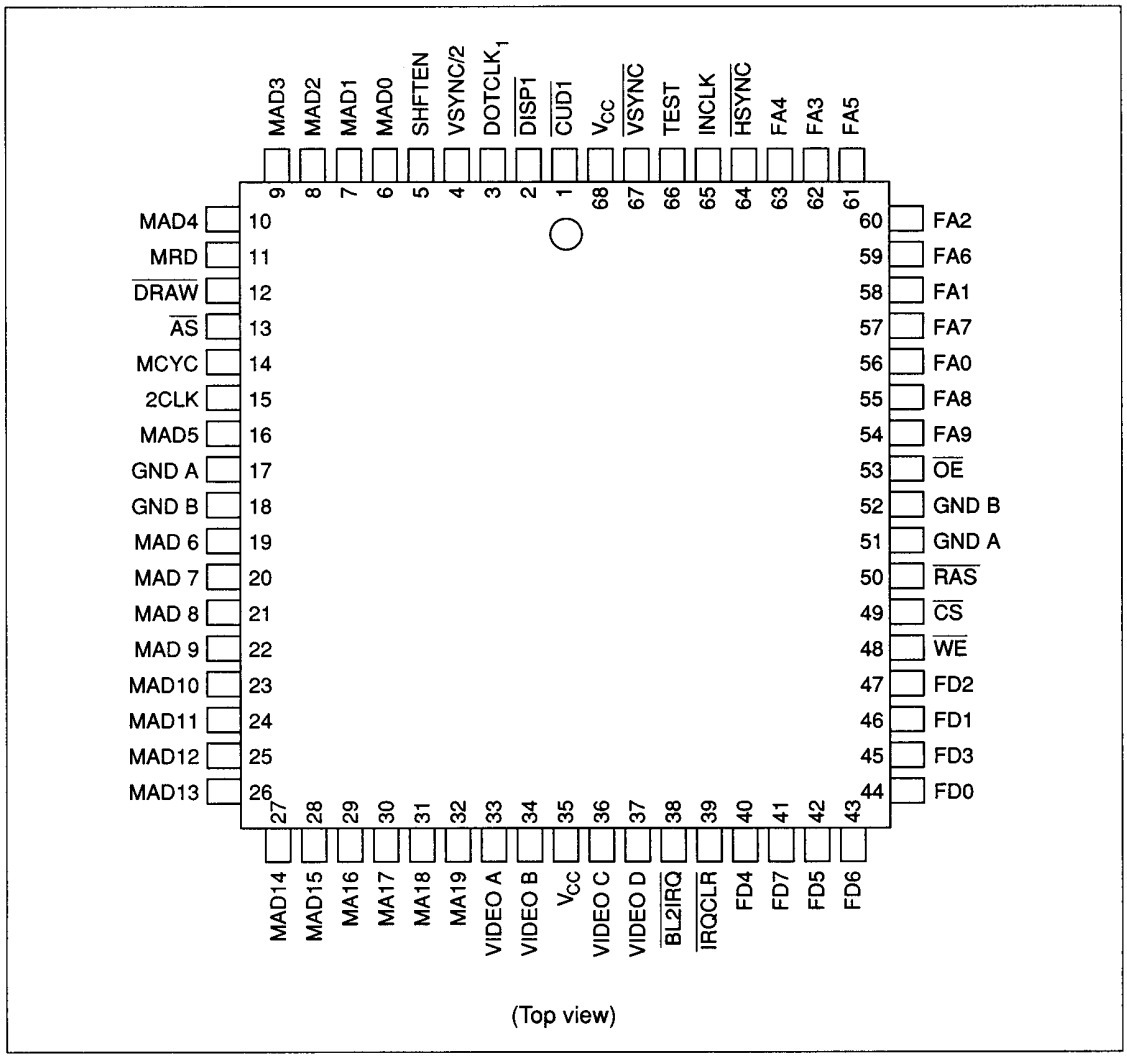
Rev. 1
Feb. 1990

The MIVAC belongs to the HD63484 ACRTC (Advanced CRT controller) family. It includes peripheral control circuits for graphic display on a chip. Incorporating bus driver circuits and a DRAM interface, the MIVAC allows direct connection to DRAMs with no external circuits. On-chip parallel/serial converting shift register generates high speed video signals. Adopting static column mode, fast memory access achieves high throughput in spite of narrow memory data bus. The MIVAC provides most functions required at peripherals of a frame buffer for graphic display constructed with 1 to 4 memory chips, and enables small size graphic system easily. Using the Hi-BiCMOS process, the MIVAC achieves high speed memory access with low power dissipation.

Features

- Directly connected with 1 to 4 memory devices (× 4 bit organization, static column mode)
- Generates DRAM interface signals: row and column address, $\overline{RAS}$, $\overline{CS}$, $\overline{OE}$, $\overline{WE}$ and memory data
- Generates high speed video signal: dot rate of 33 MHz (max)
- 16 kinds of operation modes by the combination of;
  - 2, 4 and 16 colors (1, 2 and 4 bit/pixel)
  - 8, 16 and 32 dot shift
  - Single/dual access
  - 1, 2 and 4 chips memory
- Blinking block cursor display
- Memory variation: 256 k × 4 static column mode DRAM
- Generates special clock to drive the ACRTC (asymmetrical 2CLK)
- Input clock divider to generate dot clocks (divided by 1, 2 and 4)
- Supports frame sequential application
  - $\overline{VSYNC}$ divider and VSYNC/2 output
  - 4 → 2 bit video output multiplexer
- BLINK2 interrupting control ($\overline{BL2IRQ}$ output)
- $\overline{CS}$ before $\overline{RAS}$ refresh
- Direct interface with the ACRTC
- Supports hardware window of ACRTC
- TTL compatible input/output
- Single +5 V power supply
- Low power dissipation

Pin Assignment

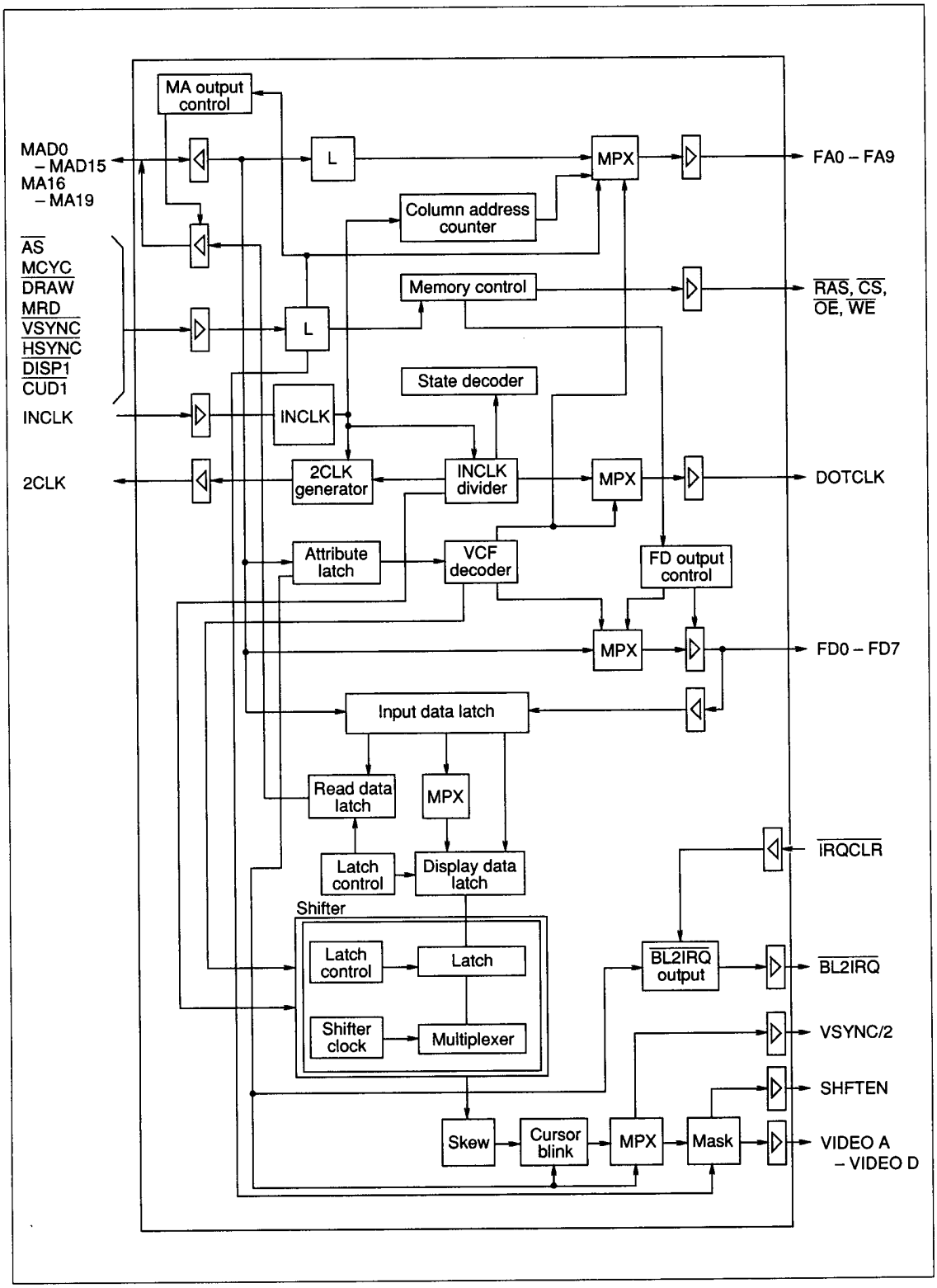


(Top view)

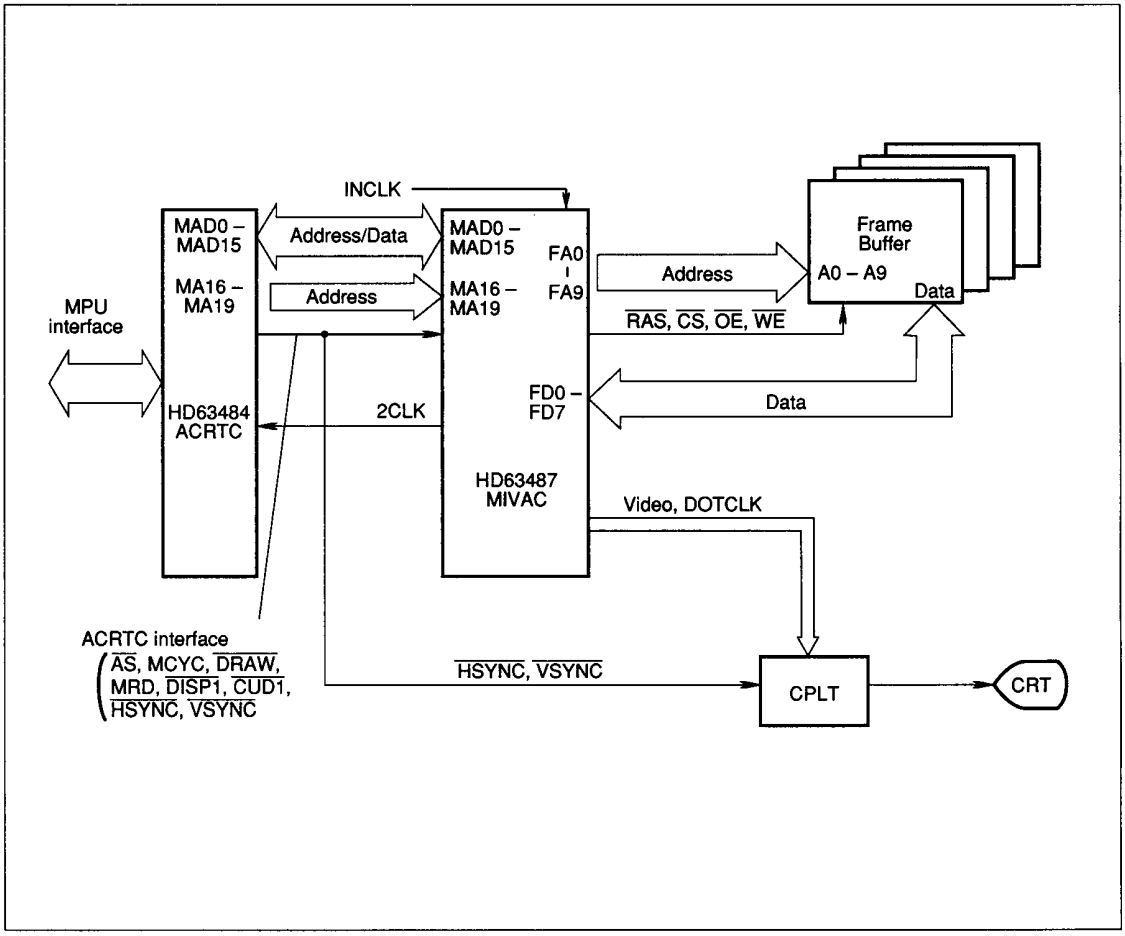
Table 1 Function Table

Mode	Attribute code (ACRTC) MAD3	MAD2	MAD1	MAD0	MCYC fetch	Access mode	Memory chip	Bit/ pixel	Shifted dot	DOTCK division
0	0	0	0	0	1	Single	1	1	16	1
1	0	0	0	1	1	Single	1	2	8	2
2	0	0	1	0	1	Single	1	4	4	4
3	0	0	1	1	1	Single	2	2	16	1
4	0	1	0	0	1	Single	2	4	8	2
5	0	1	0	1	1	Single	4	4	16	1
6	0	1	1	0	1	Dual	1	1	16	2
7	0	1	1	1	1	Dual	1	2	8	4
8	1	0	0	0	1	Dual	2	1	32	1
9	1	0	0	1	1	Dual	2	2	16	2
A	1	0	1	0	1	Dual	2	4	8	4
B	1	0	1	1	1	Dual	4	2	32	1
C	1	1	0	0	1	Dual	4	4	16	2
D	1	1	0	1	2	Single	1	2	32	1
E	1	1	1	0	2	Single	1	4	16	2
F	1	1	1	1	2	Single	2	4	32	1

Block Diagram



System Application Example



Power Supply (V_{CC}, V_{SS})

V_{SS} and V_{CC} are the MIVAC power supply pins. V_{CC} pins are +5 V ± 5% supply pins. V_{SS} are the ground pins. Be sure to connect all four V_{SS} pins to ground and both V_{CC} pins to the power supply.

Operation Control Signals

In clock (INCLK): This is basic operating clock for the MIVAC.

Test (TEST): The TEST input is used for manufacturing operational testing. It must be fixed low when the MIVAC is mounted in a system.

ACRTC Interface Signals

Clock (2CLK): The 2CLK clock output is a basic clock for the ACRTC's internal operation. The MIVAC generates 2CLK by dividing the INCLK.

Memory cycle (MCYC): The ACRTC's MCYC output supplies this input. The MCYC input indicates the ACRTC's frame buffer access timing. MCYC is low when the ACRTC is in the address cycle, and high when the ACRTC is in the data cycle.

Draw ($\overline{DRAW}$): The ACRTC's $\overline{DRAW}$ output supplies this input. The $\overline{DRAW}$ input indicates whether the ACRTC memory cycle is a drawing cycle. $\overline{DRAW}$ is low during drawing cycle, and high otherwise. The MIVAC uses $\overline{DRAW}$ to recognize display cycles, and also to generate DRAM control signals.

Memory read (MRD): The ACRTC's MRD output supplies this input. The MRD input controls data transfer between frame buffers and the ACRTC. The ACRTC pulls MRD high when it reads data from the frame buffer, and low when it writes data.

Address strobe ($\overline{AS}$): The ACRTC's $\overline{AS}$ output supplies this input. The $\overline{AS}$ input is a latch timing signal for the memory address sent from the ACRTC. Additionally, $\overline{AS}$ indicates whether memory is begun accessed.

Horizontal sync ($\overline{HSYNC}$): The ACRTC's $\overline{HSYNC}$ output supplies this input. The $\overline{HSYNC}$ input is a DRAM refresh cycle control signal to horizontally synchronize CRT displays. The MIVAC performs $\overline{CS}$ before $\overline{RAS}$ refresh when $\overline{HSYNC}$ is low and $\overline{DRAW}$ is high when AS pulses are input.

Vertical sync ($\overline{VSYNC}$): The ACRTC's output supplies this input. The MIVAC internally divides $\overline{VSYNC}$ by 2 to generate the VYNCS/2 output.

Display 1 ($\overline{DISP1}$): The ACRTC's $\overline{DISP1}$ output supplies this input. It indicates the screen's display period. Usually, the ACRTC's DSP (display signal control) bit is set to 1.

Cursor display 1 ($\overline{CUD1}$): The ACRTC's $\overline{CUD1}$ output supplies this input. It is low when the graphic cursor is display period.

Memory address/data 0 – 15 (MAD0 – MAD15): The ACRTC's MAD0 – MAD15 output supplies this input. When MCYC is low, MAD0 – MAD15 indicate the frame buffer address. When MCYC is high, they transfer the drawing data to and from the frame buffer.

Memory address 16 – 19 (MA16 – MA19): The ACRTC's address MA16 – MA19 for frame buffer access supplies this input.

Frame Buffer Access Signals

Row address strobe ($\overline{RAS}$): The MIVAC outputs the DRAM's $\overline{RAS}$ timing signal on the $\overline{RAS}$ output.

Chip select ($\overline{CS}$): The MIVAC outputs the DRAM's $\overline{CS}$ timing signal on the $\overline{CS}$ output.

Write enable ($\overline{WE}$): The MIVAC outputs the DRAM's $\overline{WE}$ timing signals on the $\overline{WE}$ outputs.

Output enable ($\overline{OE}$): The MIVAC outputs the DRAM's output timing signal on the $\overline{OE}$ output.

Frame buffer address (FA0 – FA7): The MIVAC outputs the multiplexed DRAM address on FA0 – FA7.

Frame Buffer Data (FD0 – FD7)

The 8 bits FD0 – FD7 frame buffer data I/O bus transfers data between the ACRTC and frame buffers and inputs display data from the frame buffers. In 1 chip memory mode, FD0 – FD3 is used. In 2 or 4 chips memory mode, FD0 – FD7 is used.

CRT Display Interface

Dot clock (DOTCLK): The MIVAC internally divides INCLK by 1, 2 or 4 to generate the DOTCLK output. DOTCLK division ratio depends on VCF0 – VCF3 of attribute code.

Video outputs (VIDEOA – VIDEOD): VIDEOA – VIDEOD are the four bits output from the MIVAC's parallel-to-serial conversion shift register. They are supplied during a display period specified by the display signal ($\overline{DISP}$). Which outputs are usable depends on the attribute code (VCF0 – VCF3).

Shift enable (SHFTEN): SHFTEN is active high output. This output indicates the active display period of the screen.

Vertical sync divide-by-2 (VSYNC/2): VSYNC/2 output is $\overline{VSYNC}$ signal from the ACRTC divided by two.

Others

BLINK2 interrupt ($\overline{BL2IRQ}$): This output is sat by BLINK2 (MA19) of the attribute code. $\overline{BL2IRQ}$ is low when BLINK2 is high.

BLINK2 interrupt clear ($\overline{IRQCLR}$): This input clears the $\overline{BL2IRQ}$ signal. When $\overline{IRQCLR}$ is low, $\overline{BL2IRQ}$ is clear and high.

Table 2 Pin Description

Pin No.	Signal	Description
68	V_{CC}	Power
35		
52	V_{SS}	Logic ground
51		
18		
17		
15	2CLK	Output clock to the ACRTC
14	MCYC	Memory cycle input from the ACRTC
12	$\overline{DRAW}$	Draw input from the ACRTC
11	MRD	Memory read input from the ACRTC
13	$\overline{AS}$	Address strobe input from the ACRTC

Pin Description (cont)

Pin No.	Signal	Description
6	MAD0	Multiplex frame buffer address/data to/from ACRTC
7	MAD1	
8	MAD2	
9	MAD3	
10	MAD4	
16	MAD5	
19	MAD6	
20	MAD7	
21	MAD8	
22	MAD9	
23	MAD10	
24	MAD11	
25	MAD12	
26	MAD13	
27	MAD14	
28	MAD15	
29	MA16	Memory address line 16 from the ACRTC
30	MA17	Memory address line 17 from the ACRTC
31	MA18	Memory address line 18 from the ACRTC
32	MA19	Memory address line 19 from the ACRTC
64	$\overline{\text{HSYNC}}$	Horizontal sync input from the ACRTC
67	$\overline{\text{VSYNC}}$	Vertical sync input from the ACRTC
4	VSYNC/2	Vertical sync divide-by-2 output
1	$\overline{\text{CUD1}}$	Cursor control input from the ACRTC
2	$\overline{\text{DISP1}}$	Display input from the ACRTC
50	$\overline{\text{RAS}}$	Row address strobe output to DRAM
49	$\overline{\text{CS}}$	Chip select output to DRAM
48	$\overline{\text{WE}}$	Write enable output to DRAM
53	$\overline{\text{OE}}$	Output enable output to DRAM
56	FA0	Frame buffer (memory) address output 0

Pin Description (cont)

Pin No.	Signal	Description
58	FA1	Frame buffer (memory) address output 1
60	FA2	Frame buffer (memory) address output 2
62	FA3	Frame buffer (memory) address output 3
63	FA4	Frame buffer (memory) address output 4
61	FA5	Frame buffer (memory) address output 5
59	FA6	Frame buffer (memory) address output 6
57	FA7	Frame buffer (memory) address output 7
55	FA8	Frame buffer (memory) address output 8
54	FA9	Frame buffer (memory) address output 9
44	FD0	Frame buffer data input/output line 0
46	FD1	Frame buffer data input/output line 1
47	FD2	Frame buffer data input/output line 2
45	FD3	Frame buffer data input/output line 3
40	FD4	Frame buffer data input/output line 4
42	FD5	Frame buffer data input/output line 5
43	FD6	Frame buffer data input/output line 6
41	FD7	Frame buffer data input/output line 7
65	INCLK	Main timing clock input
3	DOTCLK	DOT clock output to video circuit
33	VIDEOA	Video A output
34	VIDEOB	Video B output
36	VIDEOC	Video C output
37	VIDEOD	Video D output
66	TEST	Test pin input
5	SHFTEN	Shift enable output
38	$\overline{\text{BL2IRQ}}$	BLINK2 interrupt output
39	$\overline{\text{IRQCLR}}$	BLINK2 interrupt clear input

Operation

Basic Operating Clock

Output signals from MIVAC define INCLK which inputs to MIVAC as a basic operating clock, and input signals to MIVAC define 2CLK which is output from MIVAC as well. 2CLK, the basic operating clock of ACRTC which is output from MIVAC, is generated from INCLK. In order to save the memory access time, 2CLK is configurated unsymmetrically between the first half and the latter half of cycle times as shown below.

Frame Buffer Control

MIVAC uses the DRAM of the static column mode as a memory for the frame buffer, and reduces the number of memory used for the frame buffer by accessing the memory several times per memory cycles. Using one, two, and four DRAMs respectively, MIVAC can deal with various kinds of applications. Figure 2 shows the connection of MIVAC to the DRAM.

To control these DRAMs, MIVAC generates $\overline{RAS}$, $\overline{CS}$, $\overline{OE}$ and $\overline{WE}$. And it outputs the row and the column address as the ones for DRAM, adapting to the timing of $\overline{RAS}$ and $\overline{CS}$.

The drawing read cycle is shown in figure 3, the drawing write cycle in figure 4, the display read cycle in figure 5 and 6, and $\overline{CS}$ before $\overline{RAS}$ refresh cycle in figure 7 respectively.

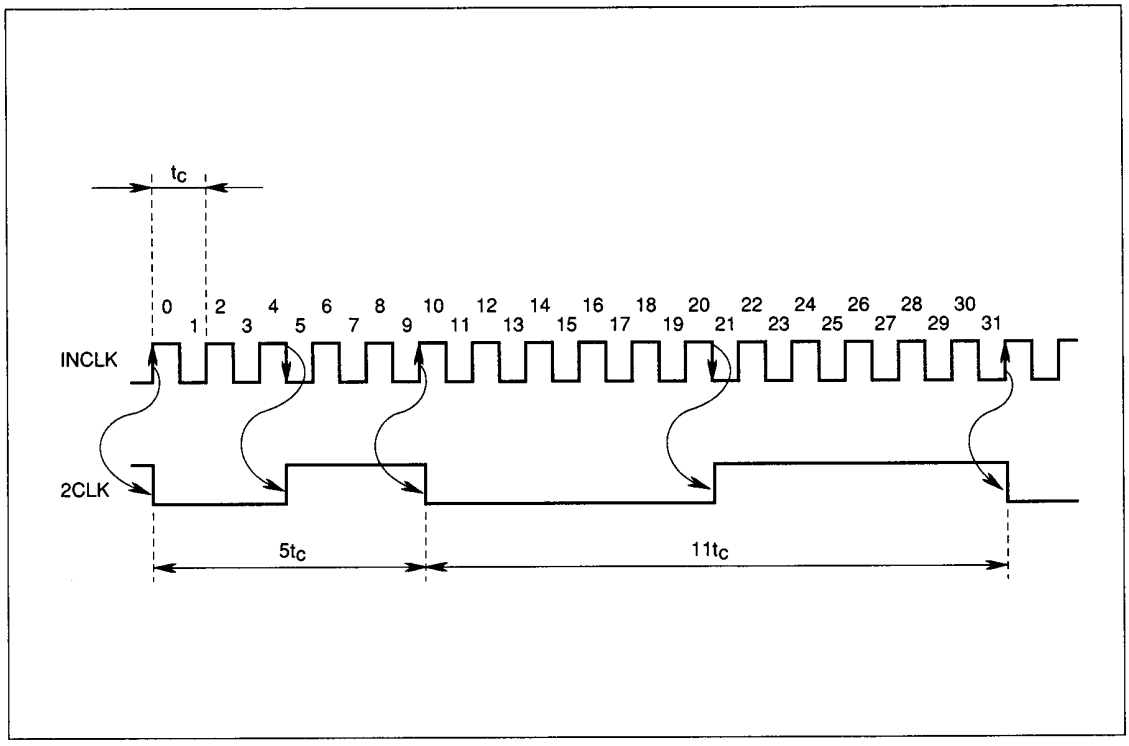
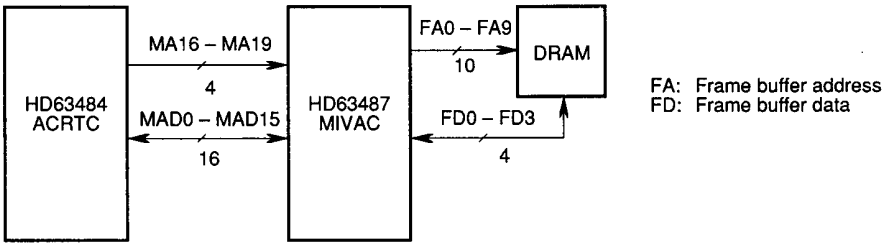
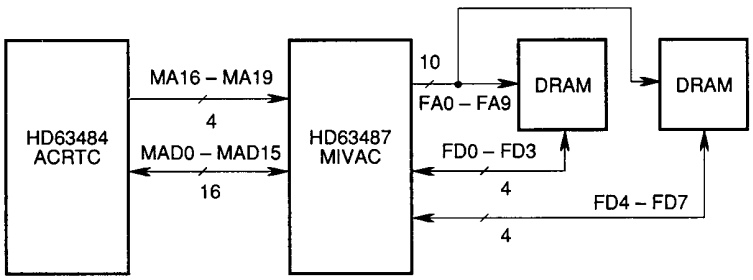


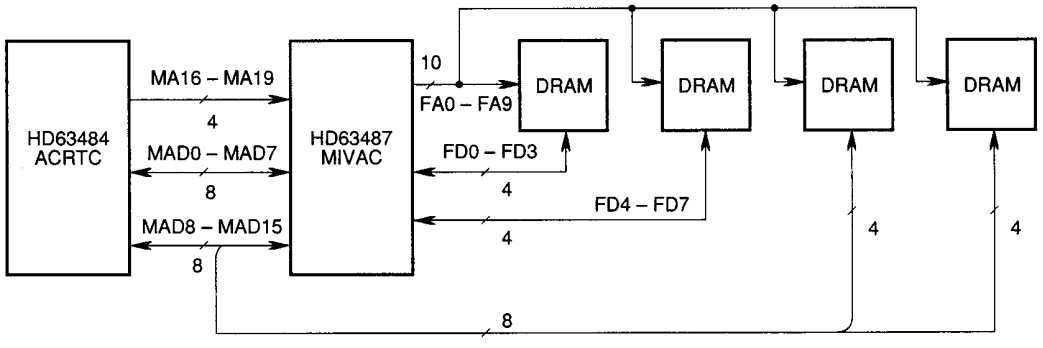
Figure 1 2CLK Output Timing



(a) 1 memory chip



(b) 2 memory chips



(c) 4 memory chips

Figure 2 Frame Buffer Connections

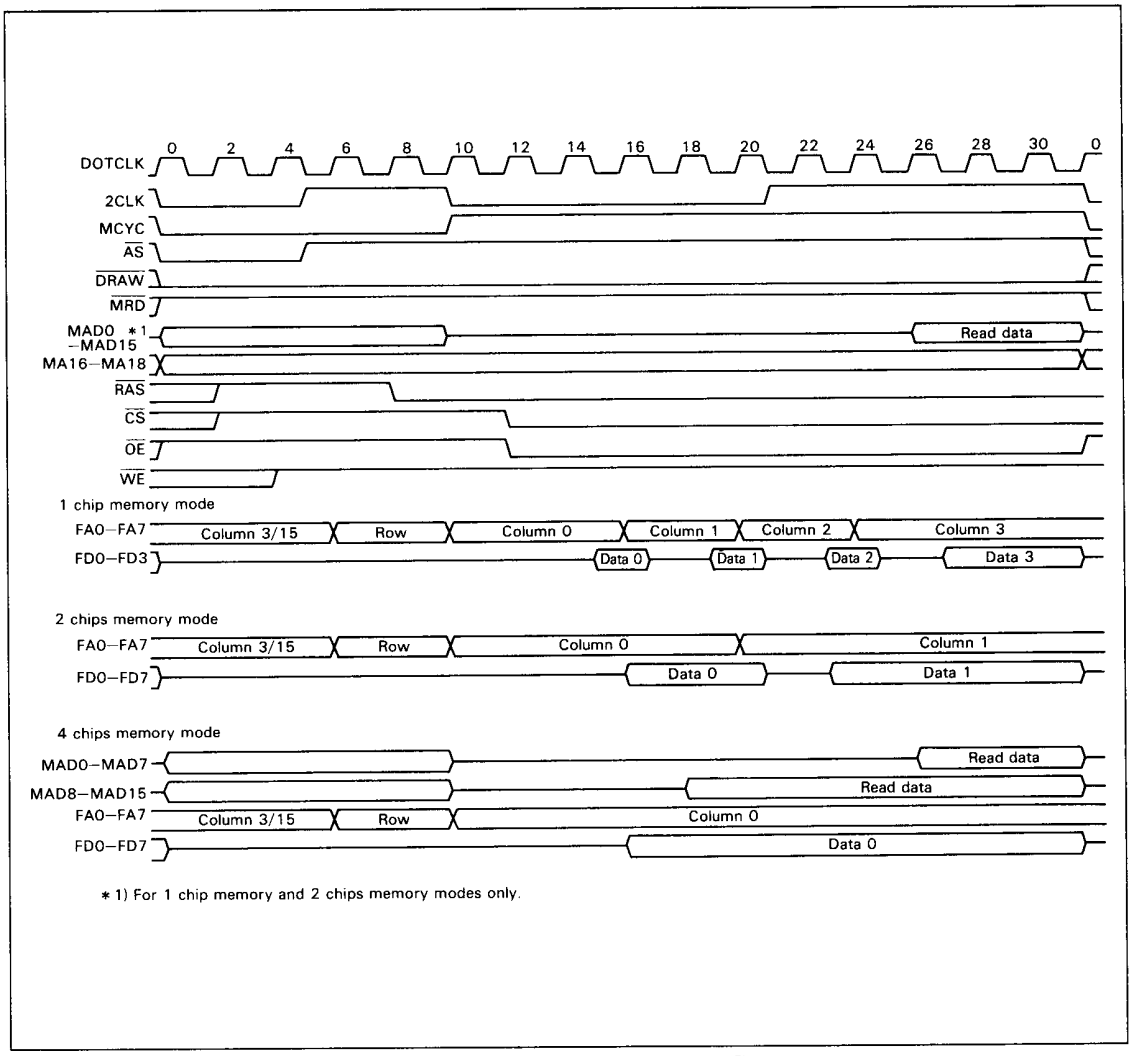


Figure 3 1MCYC Drawing Read Cycle

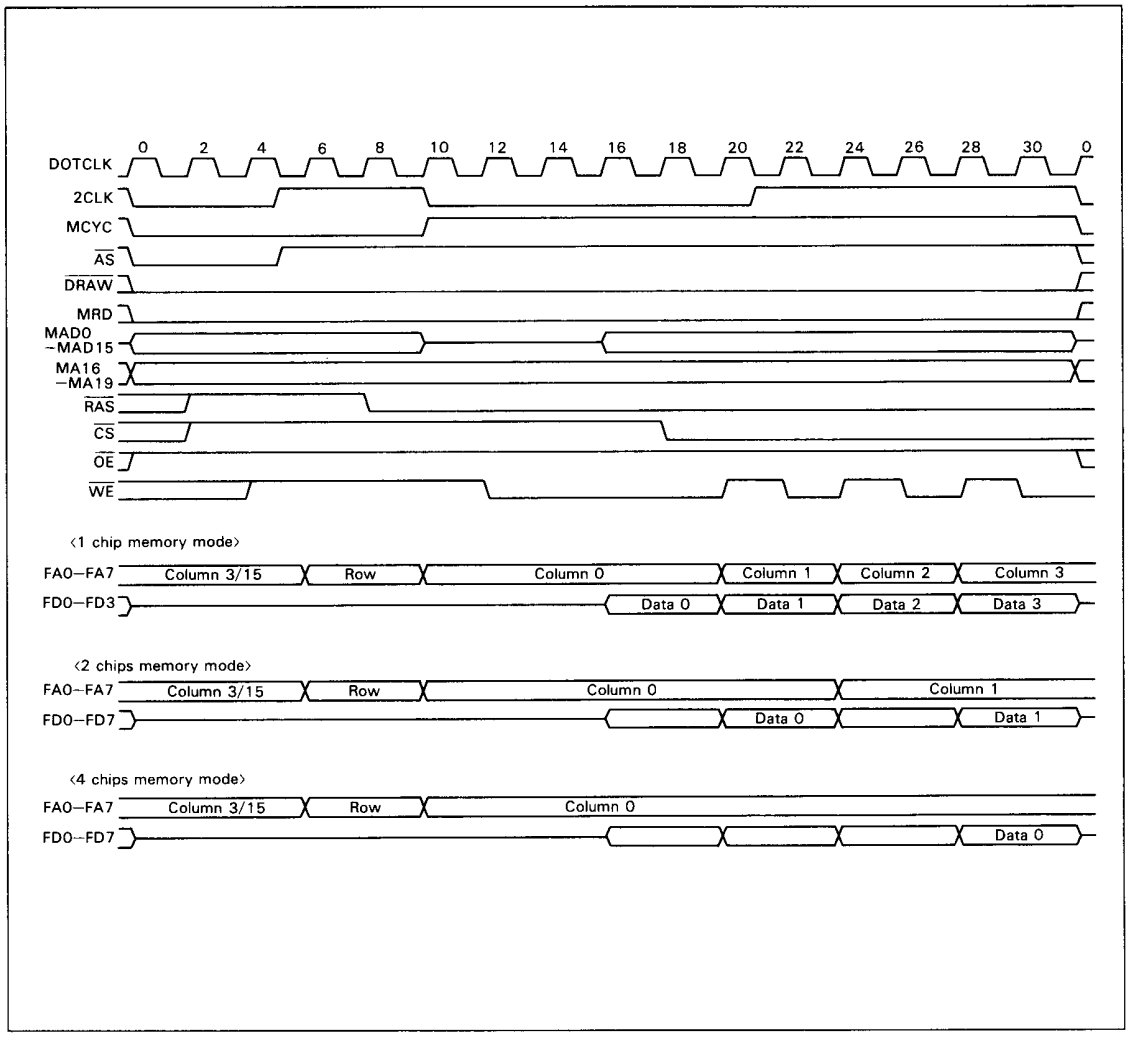


Figure 4 1MCYC Drawing Write Cycle

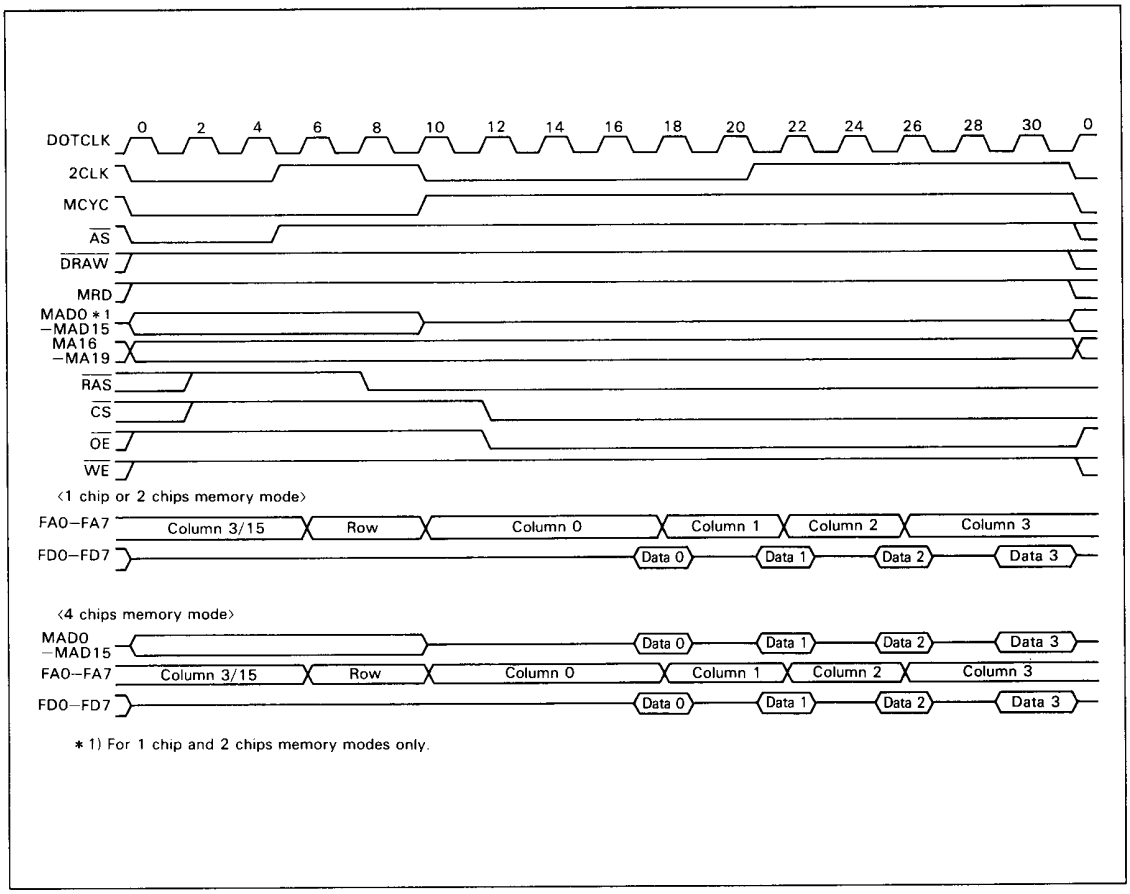


Figure 5 1MCYC Display Read Cycle

Data Transfer

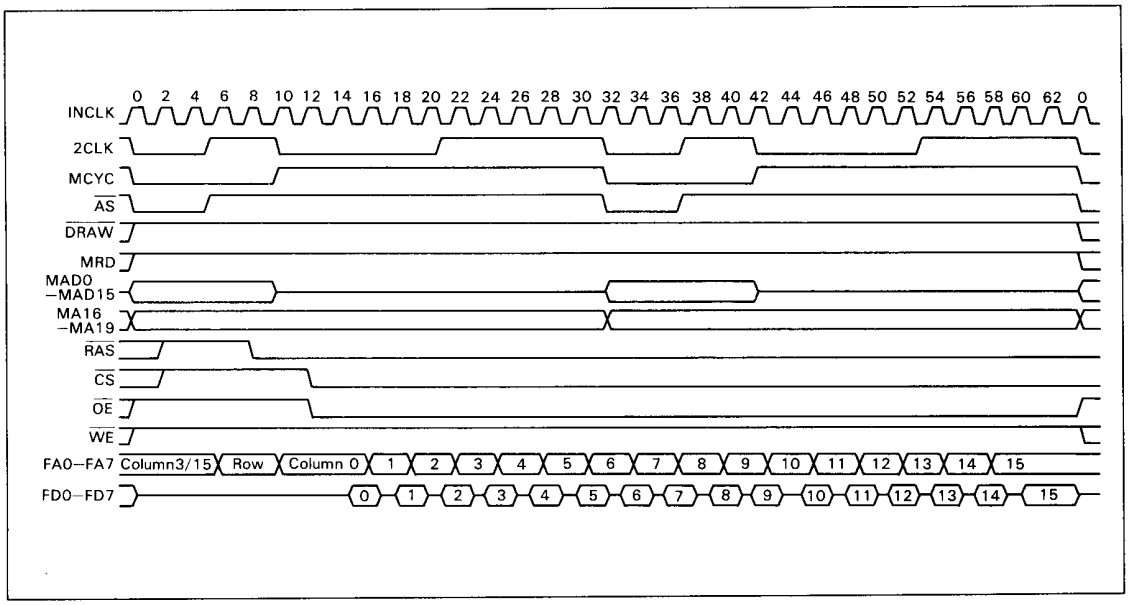


Figure 6 2MCYC Display Read Cycle

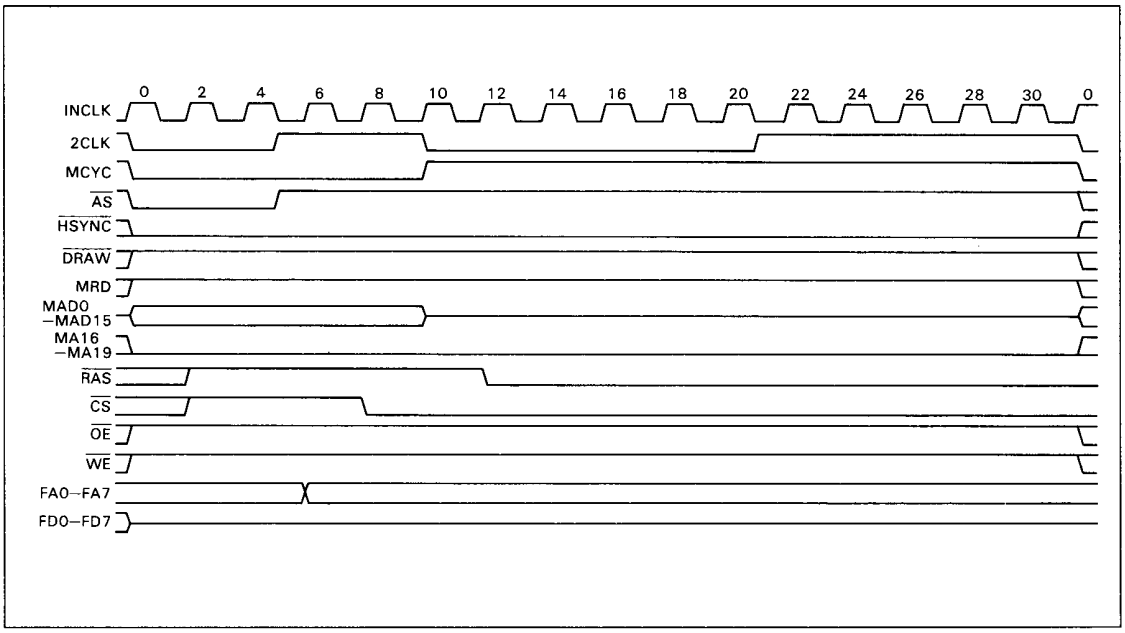


Figure 7 $\overline{CS}$ before $\overline{RAS}$ Refresh Cycle

Data Transfer

The MIVAC contain control circuits for bidirectional transfer between the ACRTC and frame buffers. To transfer data, the MIVAC receive the ACRTC's memory cycle (MCYC), memory read (MRD), draw ($\overline{DRAW}$) and address strobe ($\overline{AS}$) signals.

The MIVAC recognize a nondisplay cycle when $\overline{DRAW}$ is low. In nondisplay cycles the data transfer direction is determined by the memory read signal (MRD). MRD high signifies a read cycle to transfer data from frame buffers to the ACRTC. MRD low signifies a write cycle to transfer data from the ACRTC to the frame buffers. Timing for the data transfer is determined by the MCYC input. When MCYC is high, frame buffers or the ACRTC three-state output buffers are enabled for transfer.

Drawing write cycle: The MIVAC recognize a drawing write cycle when both $\overline{DRAW}$ and MRD are low.

Drawing read cycle: The MIVAC recognize a drawing read cycle when $\overline{DRAW}$ is low and MRD is high.

When MCYC is high during this cycle, the MIVAC enable the data buffer (MAD0 – MAD15) for the ACRTC and output a word from the frame buffers.

Video Signal Generation

MIVAC converts the parallel display data, which is output from the frame buffer, to serial in the internal shift register, and outputs the display data from VIDEOA – VIDEOD pins after making it simultaneous with DOTCLK. As the pins for VIDEOA – VIDEOD are determined by the graphic bit mode, they must be connected to CRT carefully. Table 3 shows the relation between the mode and the used pins.

Figure 8 shows the relation between the memory access and the video output.

Table 3 Operation Mode and Video Outputs

Mode	Graphic bit mode (bit/pixel)	Display colors (or gray scale)	VIDEOA	VIDEOB	VIDEOC	VIDEOD
0	1	Monochrome (2)	○	×	×	×
1	2	4 (4)	○	○	×	×
2	4	16 (16)	○	○	○	○
3	2	4 (4)	○	○	×	×
4	4	16 (16)	○	○	○	○
5	4	16 (16)	○	○	○	○
6	1	Monochrome (2)	○	×	×	×
7	2	4 (4)	○	○	×	×
8	1	Monochrome (2)	○	×	×	×
9	2	4 (4)	○	○	×	×
A	4	16 (16)	○	○	○	○
B	2	4 (4)	○	○	×	×
C	4	16 (16)	○	○	○	○
D	2	4 (4)	○	○	×	×
E	4	16 (16)	○	○	○	○
F	4	16 (16)	○	○	○	○

○: Available
×: Not available

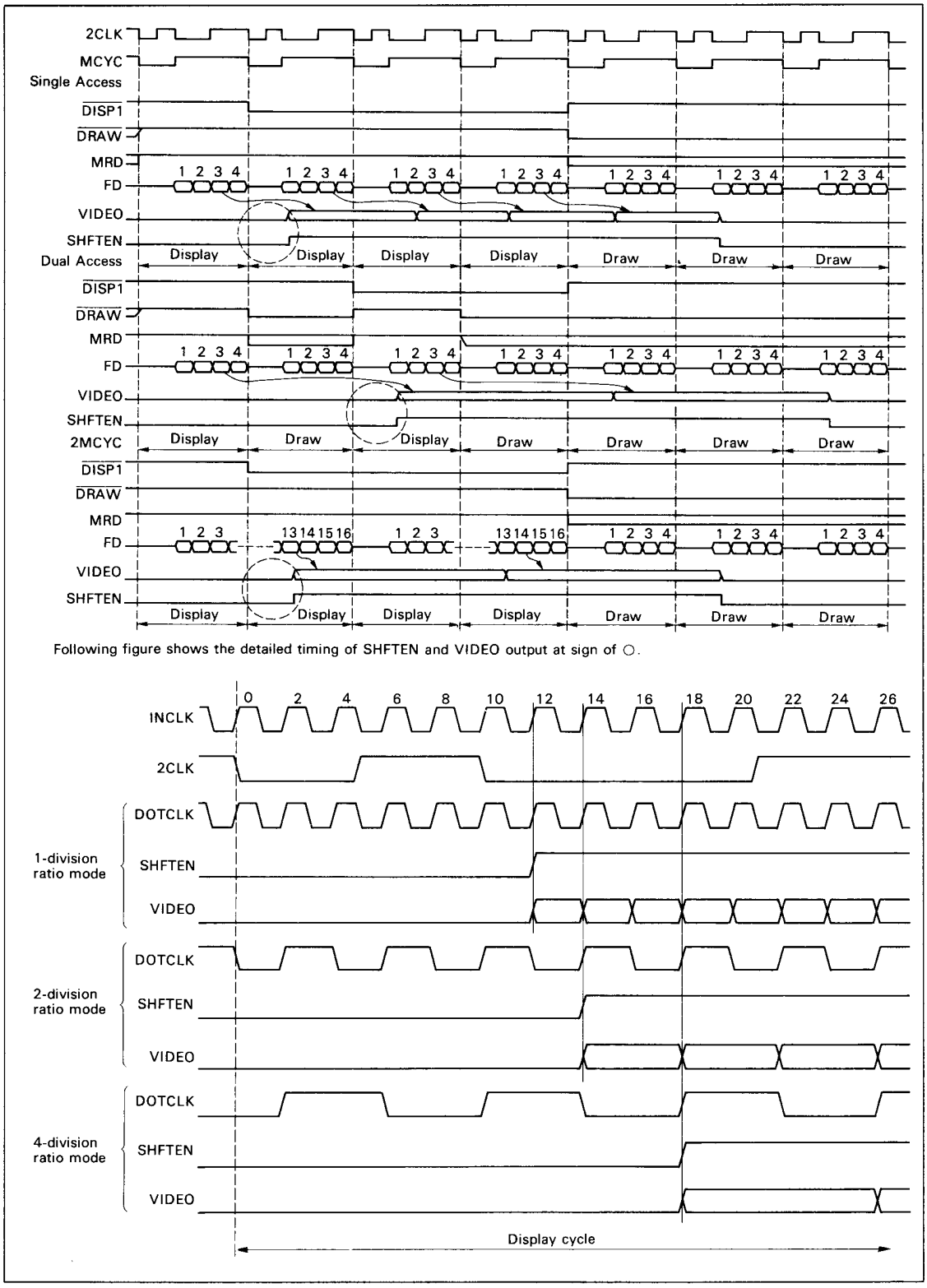


Figure 8 Display Timing (Single Access, Dual Access, 2MCYC)

Attribute Control Codes

The MIVAC sets colors, the number of shift bits, and access mode when it receives attribute codes and blink information from the ACRTC. The ACRTC outputs 20 bits of attribute control codes (MAD0 to MAD15, MA16 and MA19) during the attribute control code output cycle (figure 9). This information includes user-definable codes and blink control codes (figure 10).

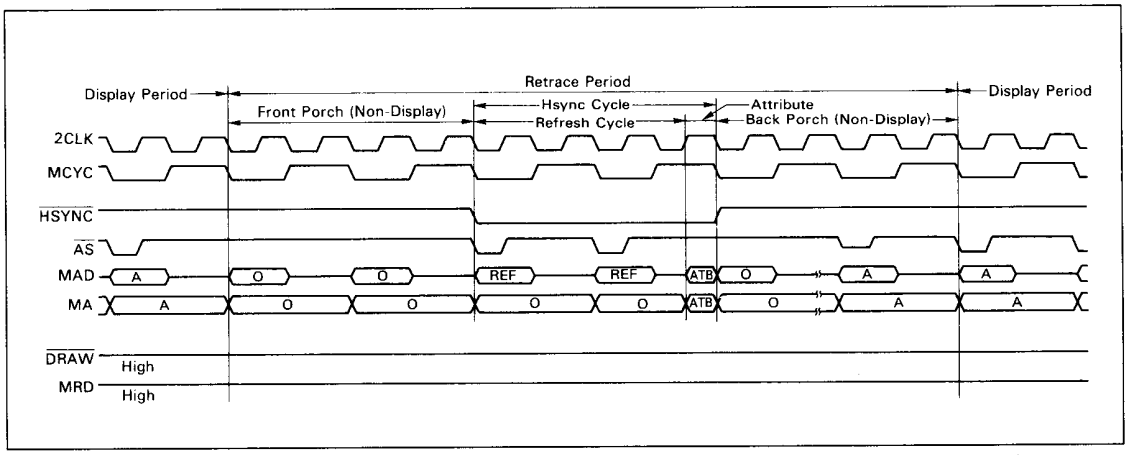


Figure 9 DRAM Refresh and Attribute Code Output Timing (Single Access Mode)

Signal	Attribute Control Codes	
MA19	BLINK2	BL2IRQ output
MA18	BLINK1	Graphic cursor cursor blinking
MA17	SPL2	
MA16	SPL1	
MAD15	HZ3	
⎛	⎛	
MAD12	HZ0	MIVAC does not use
MAD11	HSD3	
⎛	⎛	
MAD8	HSD0	
MAD7	MUXEN	Video multiplex output enable
MAD6	VMD	Frame buffer depth
MAD5	CUR1	Color of graphic cursor
MAD4	CUR0	
MAD3	VCF3	MIVAC operating modes
MAD2	VCF2	Attribute Control Codes
MAD1	VCF1	
MAD0	VCF0	

Figure 10 Attribute Control Codes

VCF0 – VCF3 (MAD0 – MAD3)

VCF0 to VCF3 (MAD0 to MAD3) define sixteen basic operating modes as shown in the tables 4 and 5.

Table 4 Operating Modes

Mode	ACRTC attribute code setting VCF3	VCF2	VCF1	VCF0	Screen configuration (dots × rasters)	Frame buffer (bytes)	ACRTC Operating frequency (MHz)	Memory access	Access mode	Memory chips	Color gradation	Shift (bits)	DOTCLK Division ratio	DOTCLK Maximum frequency (MHz)
0	0	0	0	0	640 × 200, 350, 400, 480	512 k/128 k	4.13	480 ns/ 4 times	Single access mode	1	B & W	16	1	33
1	0	0	0	1	640 × 200, 480 × 240, 320 × 200, 240						4	8	2	16.5
2	0	0	1	0	320 × 200, 240 256 × 192						16	4	4	8.25
3	0	0	1	1	640 × 200, 350, 400, 480	1 M/256 k				2	4	16	1	33
4	0	1	0	0	640 × 200 480 × 240, 320 × 200, 240						16	8	2	16.5
5	0	1	0	1	640 × 200, 350, 400, 480	2 M/512 k				4		16	1	33
6	0	1	1	0	640 × 200, 480 × 240, 320 × 200, 240	512 k/128 k			Dual access mode 0	1	B & W		2	16.5
7	0	1	1	1	320 × 200, 240 256 × 192						4	8	4	8.25
8	1	0	0	0	640 × 200, 350, 400, 480	1 M/256 k				2	B & W	32	1	33
9	1	0	0	1	640 × 200, 480 × 240, 320 × 200, 240						4	16	2	16.5
A	1	0	1	0	320 × 200, 240 256 × 192						16	8	4	8.25
B	1	0	1	1	640 × 200, 350, 400, 480	2 M/512 k				4	4	32	1	33
C	1	1	0	0	640 × 200, 480 × 240, 320 × 200, 240						16	16	2	16.5
D	1	1	0	1	640 × 200, 350, 400, 480	512 k/128 k		960 ns/ 16 times	Single access mode	1	4	32	1	33
E	1	1	1	0	640 × 200, 480 × 240, 320 × 200, 240						16	16	2	16.5
F	1	1	1	1	640 × 200, 350, 400, 480	1 M/256 k				2		32	1	33

Table 5 Dot Clock Frequency Range

Mode	Frequency
0, 3, 5, 8, B, D, F	33 – 11 MHz
1, 4, 6, 9, C, E	16.5 – 5.5 MHz
2, 7, A	8.25 – 2.75 MHz

MCYC fetch: The MCYC fetch defines the number of cycles.

1: One, two, or four memories
2: One or two memories

Access mode: The MIVAC supports signle- and dual-access 0 modes.

1: Single access/dual access 0
2: Single access

Memory chips: The MIVAC can connect one, two, or four memory chips.

1 chip: connect FD0 to FD3 to data bus
2 chips: connect FD0 to FD8 to data bus
3 chips: connect FD0 to FD7 to low-order 8 bits, and MAD8 to MAD15 to high-order 8 bits of data bus.

Bit/pixel: The MIVAC can display:

- 1 bit/pixel (B and W)
- 2 bits/pixel (4 colors)
- 4 bits/pixel (16 colors)

Dot shift: The MIVAC can shift by 4, 8, 16, or 32 dots.

DOTCLK division: The MIVAC can divide the INCLK frequency by 1, 2 or 4 depending on the number of shifted dots and access modes.

CUR0 and CUR1 (MAD4 and MAD5)

CUR0 and CUR1 set the cursor color (table 6).

VMD0 (MAD6)

VMD0 selects memory chips (table 7).

MUXEN (MAD7)

MUXEN selects the multiplex video output. Multiplexing is defined by MUXEN and VSYNC/2 (table 8). VSYNC/2 is obtained by dividing $\overline{\text{VSYNC}}$ from the ACRTC by 2.

Note: VIDEOD is not multiplexed.

BLINK1 (MA18)

BLINK1 defines the blinking of cursor (table 9).

BLINK2 (MA19)

BLINK2 controls $\overline{\text{BL2IRQ}}$ output. When BLINK2 is 1, $\overline{\text{BL2IRQ}}$ is asserted (low).

Table 6 Cursor Color

CUR1	CUR0	Cursor color
0	0	Black (VIDEOA to VIDEOD = 0)
0	1	White (VIDEOA to VIDEOD = 1)
1	0	Color specified by each bit (VIDEOA to VIDEOD) is inverted.
1	1	Color specified by each bit (VIDEOA to VIDEOC) is inverted. (VIDEOD is not changed.)

Table 7 Memory Chips

VMD	Memory chips
0	256 k words × 4 bit DRAM
1	1 M words × 4 bit DRAMs

Table 8 Video Multiplex

MUXEN	VSYNC/2	VIDEOA	VIDEOB
0	0	A	B
	1	A	B
1	0	A	B
	1	C	D

Table 9 Cursor Blink

BLINK1	Cursor
0	No blinking
1	Blinking

Table 10 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	V_{CC} (Note)	–0.3 to +7.0	V
Input voltage	Vin (Note)	–0.3 to V_{CC} + 0.3	V
Output Voltage	Vout (Note)	5.5	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +150	°C

Note: This value is in reference to V_{SS} = 0 V.

Table 11 Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC} (Note)	4.75	5.00	5.25	V
Input "Low" level voltage	V_{IL} (Note)	0	—	0.7	V
Input "High" level voltage	V_{IH} (Note)	2.2	—	V_{CC}	V
Operating temperature	Topr	0	25	70	°C

Note: This value is in reference to V_{SS} = 0 V.

Electrical Characteristics

Table 12 DC Characteristics (V_{CC} = 5.0 V ± 5%, V_{SS} = 0 V, Ta = 0 to +70°C unless otherwise noted.)

Item		Symbol	Min	Max	Unit	Test condition
Input "High" level voltage	All inputs	V_{IH}	2.2	V_{CC}	V	
Input "Low" level voltage	All inputs	V_{IL}	–0.3	0.7	V	
Input clamp voltage	All inputs	V_I	—	–1.5	V	V_{CC} = 4.75 V Iin = 18 mA
Output "High" level voltage	All outputs	V_{OH}	2.7	—	V	V_{CC} = 4.75 V I_{OH} = –400 µA
Output "Low" level voltage	All outputs	V_{OL}	—	0.5	V	V_{CC} = 4.75 V I_{OL} = 8 mA
"High" level input current	All inputs	I_{IH}	—	20	µA	V_{CC} = 5.25 V V_I = 2.7 V
"Low" level input current	All inputs	I_{IL}	—	–400	µA	V_{CC} = 5.25 V V_I = 0.4 V
Short circuit output current	All outputs	I_{OS}	–40	–120	mA	V_{CC} = 5.25 V
Supply current		I_{CC}	—	120	mA	V_{CC} = 5.25 V

Table 13 AC Characteristics (V_{CC} = 5.0 V ± 5%, V_{SS} = 0 V, Ta = 0 to +70°C unless otherwise noted.)

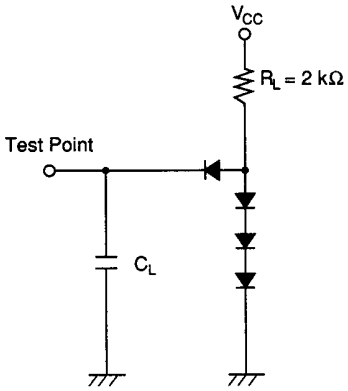
No.	Item	Symbol	Reference figure no.	Min	Max	Unit
1	INCLK cycle time	t_C	11	30	—	ns
2	INCLK high level pulse width	t_{WH}	11	12	—	ns
3	INCLK low level pulse width	t_{LW}	11	12	—	ns
4	INCLK rise time	t_R	11	—	5	ns
5	INCLK fall time	t_F	11	—	5	ns
6	2CLK delay time	t_{2CLKD}	11	—	15	ns
7	MCYC setup time	t_{MCYCS}	11	10	—	ns
8	MCYC hold time	t_{MCYCH}	11	0	—	ns
9	$\overline{\text{HSYNC}}$ setup time	t_{HSS}	11	15	—	ns
10	$\overline{\text{HSYNC}}$ hold time	t_{HSH}	11	0	—	ns
11	$\overline{\text{DISP1}}$ setup time	t_{DISPS}	11	20	—	ns
12	MRD setup time	t_{MRDS}	11	15	—	ns
13	MRD hold time	t_{MRDH}	11	5	—	ns
14	$\overline{\text{DRAW}}$ setup time	t_{DRAWS}	11	15	—	ns
15	$\overline{\text{DRAW}}$ hold time	t_{DRAWH}	11	5	—	ns
16	$\overline{\text{AS}}$ setup time	t_{ASS}	11	20	—	ns
17	$\overline{\text{AS}}$ pulse width	t_{ASW}	11	25	—	ns
18	Memory address setup time	t_{AS}	11	25	—	ns
19	Memory address hold time	t_{AH}	11	0	—	ns
20	$\overline{\text{CUD1}}$ setup time	t_{CUDS}	11	5	—	ns
21	$\overline{\text{VSYNC}}$ setup time	t_{VSS1}	17	5	—	ns
22	Attribute code delay time	t_{ACS}	20	—	100	ns
23	Attribute code hold time	t_{ASH}	20	5	—	ns
24	$\overline{\text{RAS}}$ delay time	t_{RSD}	11	—	15	ns
25	$\overline{\text{RAS}}$ precharge time	t_{RSP}	11	3tc–10	—	ns
26	$\overline{\text{CS}}$ delay time 1	t_{CSDL}	11	—	15	ns
27	$\overline{\text{OE}}$ delay time 1	t_{OED1}	11	—	15	ns
28	2CLK delay time from $\overline{\text{OE}}$	t_{2CKD}	11	0	10	ns
29	Valid MAD0 – MA19 to valid low address delay time	t_{RAD}	11	—	25	ns

AC Characteristics (V_{CC} = 5.0 V ± 5%, V_{SS} = 0 V, Ta = 0 to +70°C unless otherwise noted.) (cont)

No.	Item	Symbol	Reference figure no.	Min	Max	Unit
30	Column address delay time	t_{CAD}	11	5	25	ns
31	FD setup time	t_{FDS}	11	8	—	ns
32	FD hold time 1	t_{FDH1}	11	5	—	ns
33	FD hold time 2	t_{FDH2}	11	2	—	ns
34	Valid FD to valid MAD delay	t_{MADV}	11	—	10	ns
35	Read data turn on time	t_{RDTV}	11	0	—	ns
36	Read data hold time	t_{RDH}	11	3	—	ns
37	$\overline{WE}$ delay time	t_{WED}	14	—	25	ns
38	$\overline{WE}$ low pulse width	t_{WLW}	14	tc – 15	—	ns
39	$\overline{WE}$ high pulse width	t_{WHW}	14	tc – 15	—	ns
40	$\overline{CE}$ low to $\overline{WE}$ pulse width	t_{CWEW}	14	tc – 15	—	ns
41	Draw write data setup time	t_{WDS}	14	15	—	ns
42	FD delay time 1	t_{FDD1}	14	—	20	ns
43	FD delay time 2	t_{FDD2}	14	—	20	ns
44	$\overline{WE}$/$\overline{CS}$ low to FD hold time	t_{WFDHW}	14	tc – 10	—	ns
45	$\overline{WE}$/$\overline{CS}$ low to address hold	t_{WAHW}	14	tc – 5	—	ns
46	FD hold time	t_{FDHW}	14	0	—	ns
47	FD turn off time	t_{FDTI}	14	—	50	ns
48	VSYNC/2 delay time	t_{VS2D}	11	—	25	ns
49	DOTCLK delay time	t_{DCD}	11	—	15	ns
50	VIDEO delay time	t_{VD}	11	–5	5	ns
51	$\overline{BL2IRQ}$ delay time	t_{IRQD}	20	—	10	ns
52	$\overline{IRQCLR}$ to $\overline{BL2IRQ}$ clear delay time	t_{IRQCD}	20	—	20	ns
53	SHFTEN delay time	t_{SFTEND}	11	–5	5	ns

Test Circuit

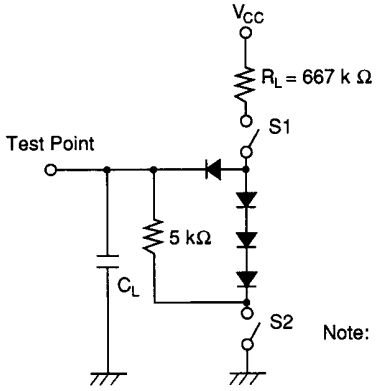
(a) Totem pole output



Note: All diodes are 1S2074Ⓗ's or the equivalent.

Signal	C_L (pF)
2CLK	40
DOTCK	
VSYNC/2	
$\overline{RAS}$	
$\overline{CS}$	
$\overline{WE}$	
$\overline{OE}$	
FA0 – FA9	
VIDEOA – VIDEOD	
SHFTEN	
$\overline{BL2IRQ}$	

(b) Three state output



Note: All diodes are 1S2074Ⓗ's or the equivalent.

Signal	C_L (pF)
MAD0 – MAD15	40
FD0 – FD7	

Table 14 Reference

Display data fetch	Memory chip	Cycle mode	Figure no.
4 fetch/1 MCYC	1 chip	Drawing read cycle	11
		Drawing write cycle	14
		Display cycle	17
		Refresh and attribute cycle	20
	2 chips	Drawing read cycle	12
		Drawing write cycle	15
		Display cycle	17
		Refresh and attribute cycle	20
	4 chips	Drawing read cycle	13
		Drawing write cycle	16
		Display cycle	18
		Refresh and attribute cycle	20
16 fetch/2 MCYC	1 chip	Drawing read cycle	11
		Drawing write cycle	14
		Display cycle	19
		Refresh and attribute cycle	20
	2 chips	Drawing read cycle	12
		Drawing write cycle	15
		Display cycle	19
		Refresh and attribute cycle	20

Timing Chart

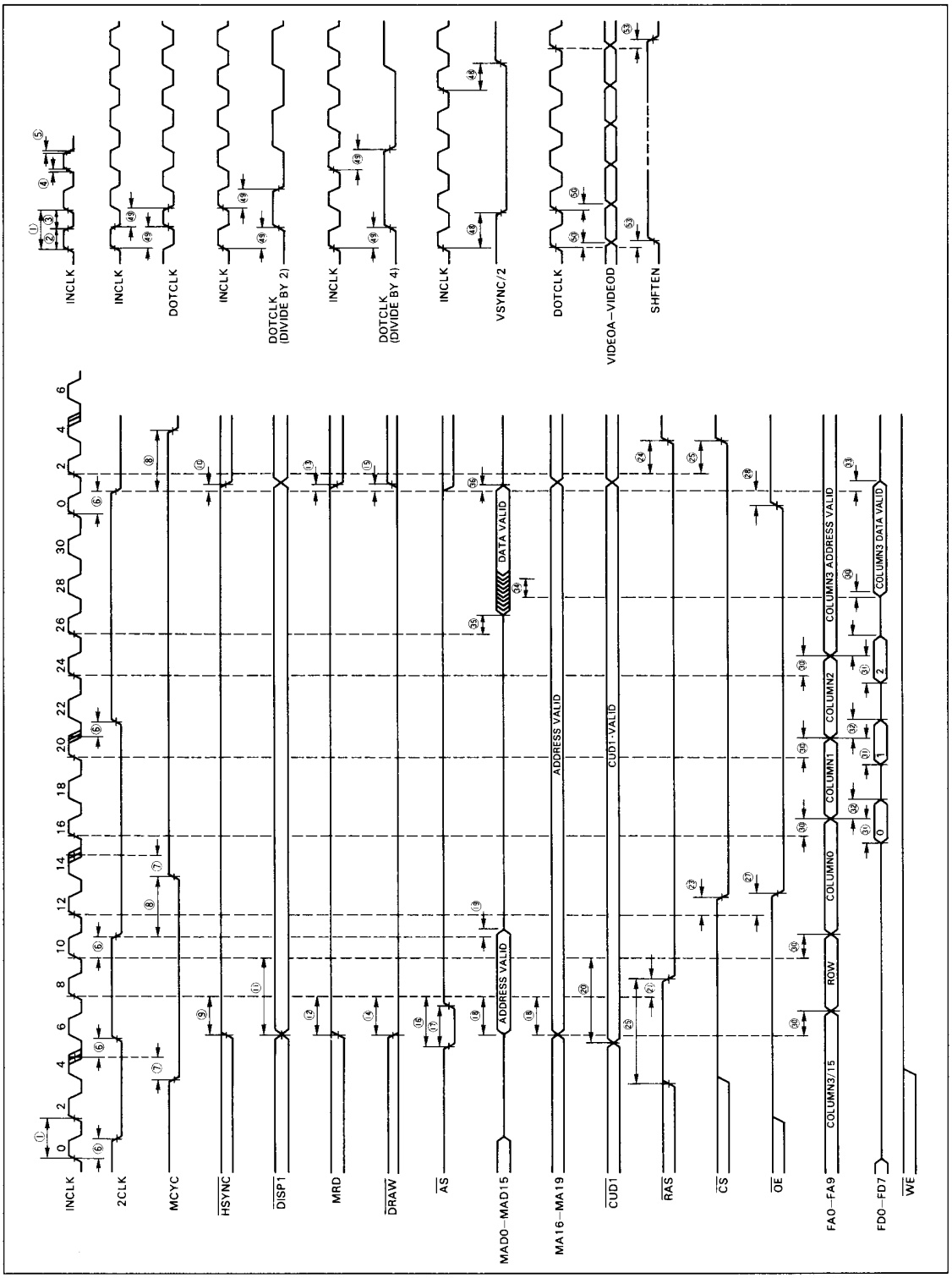


Figure 11 1MCYC Draw Read (1 Chip)

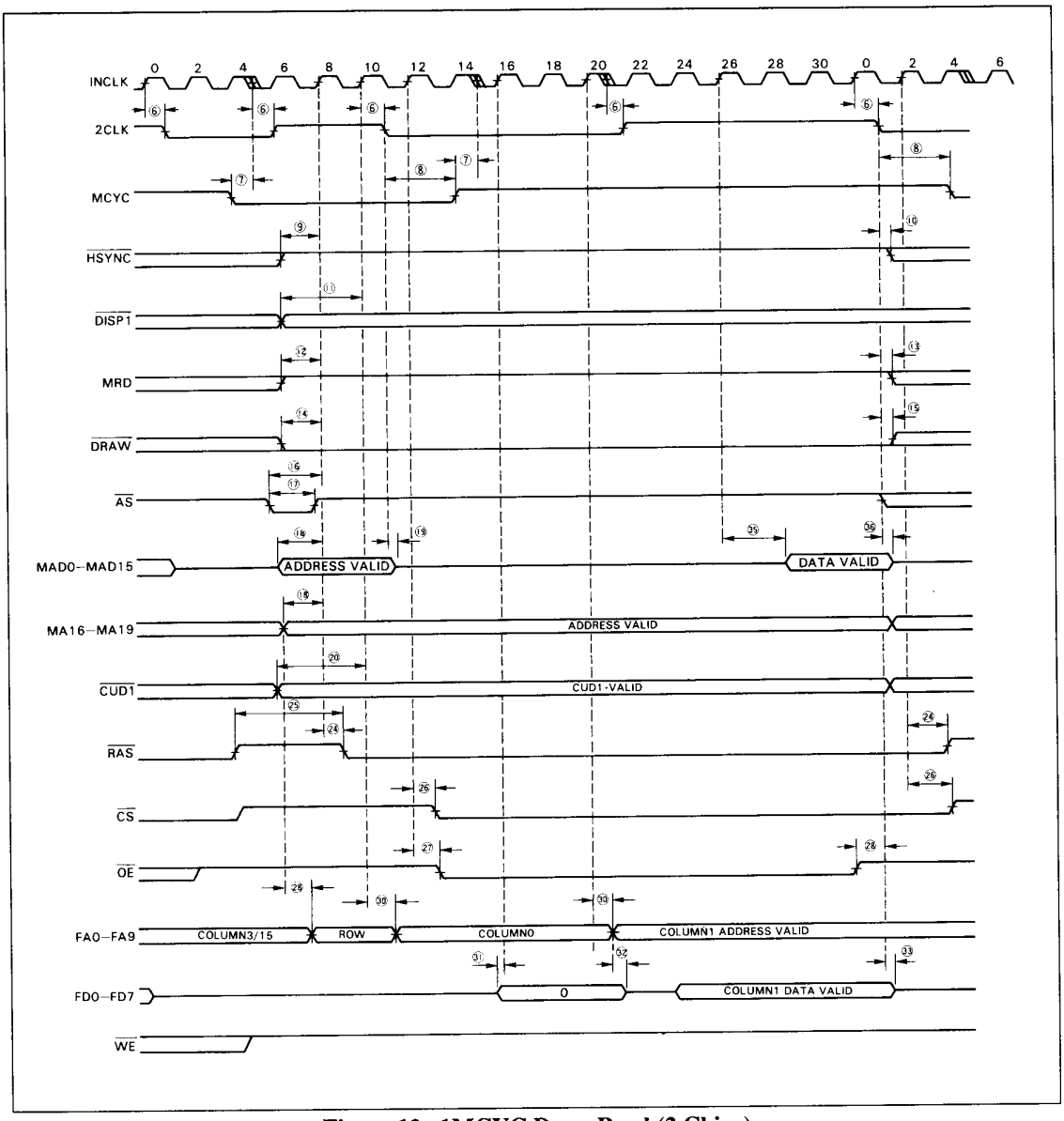


Figure 12 1MCYC Draw Read (2 Chips)

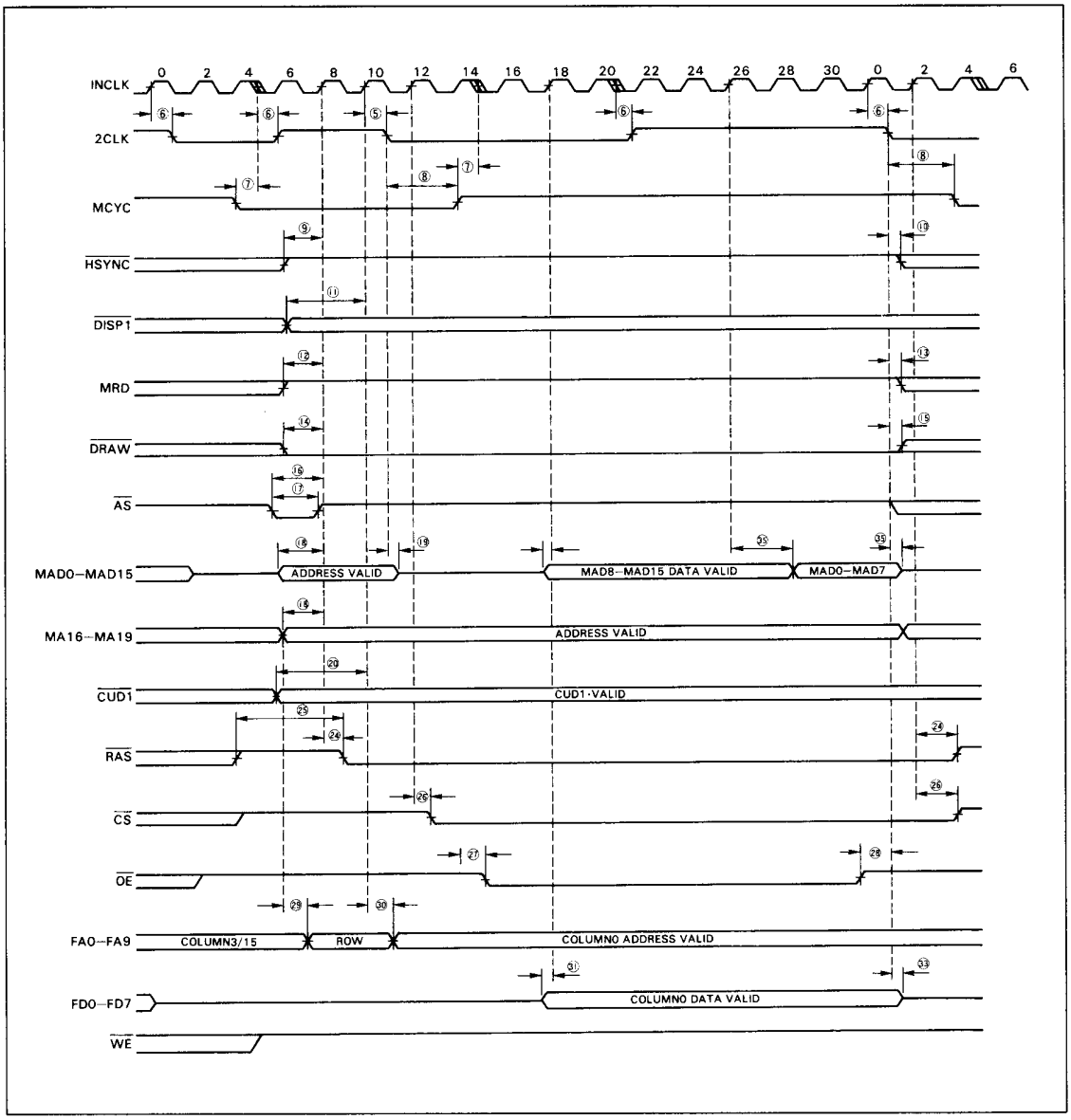


Figure 13 1MCYC Draw Read (4 Chips)

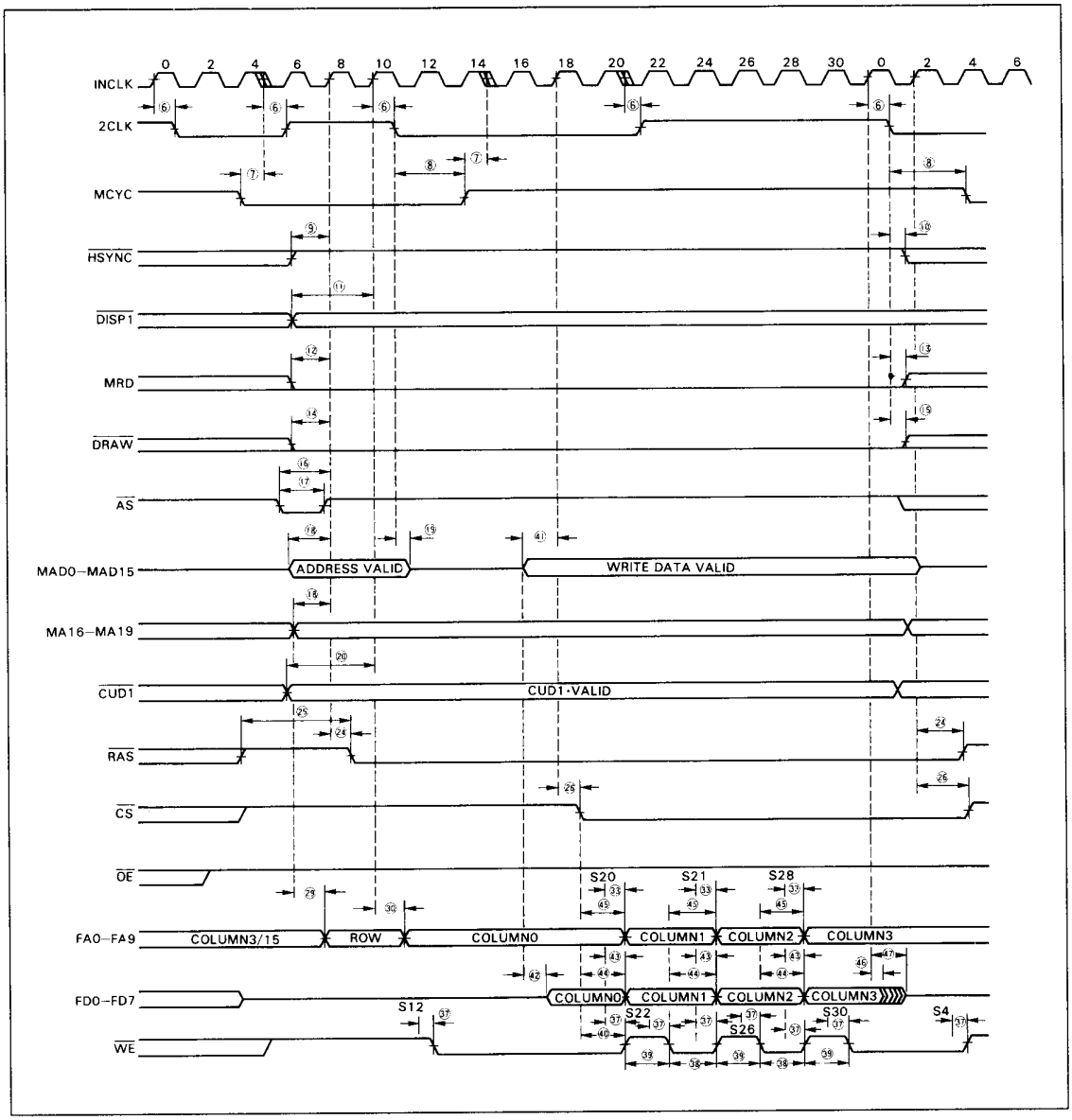


Figure 14 1MCYC Draw Write (1 Chip)

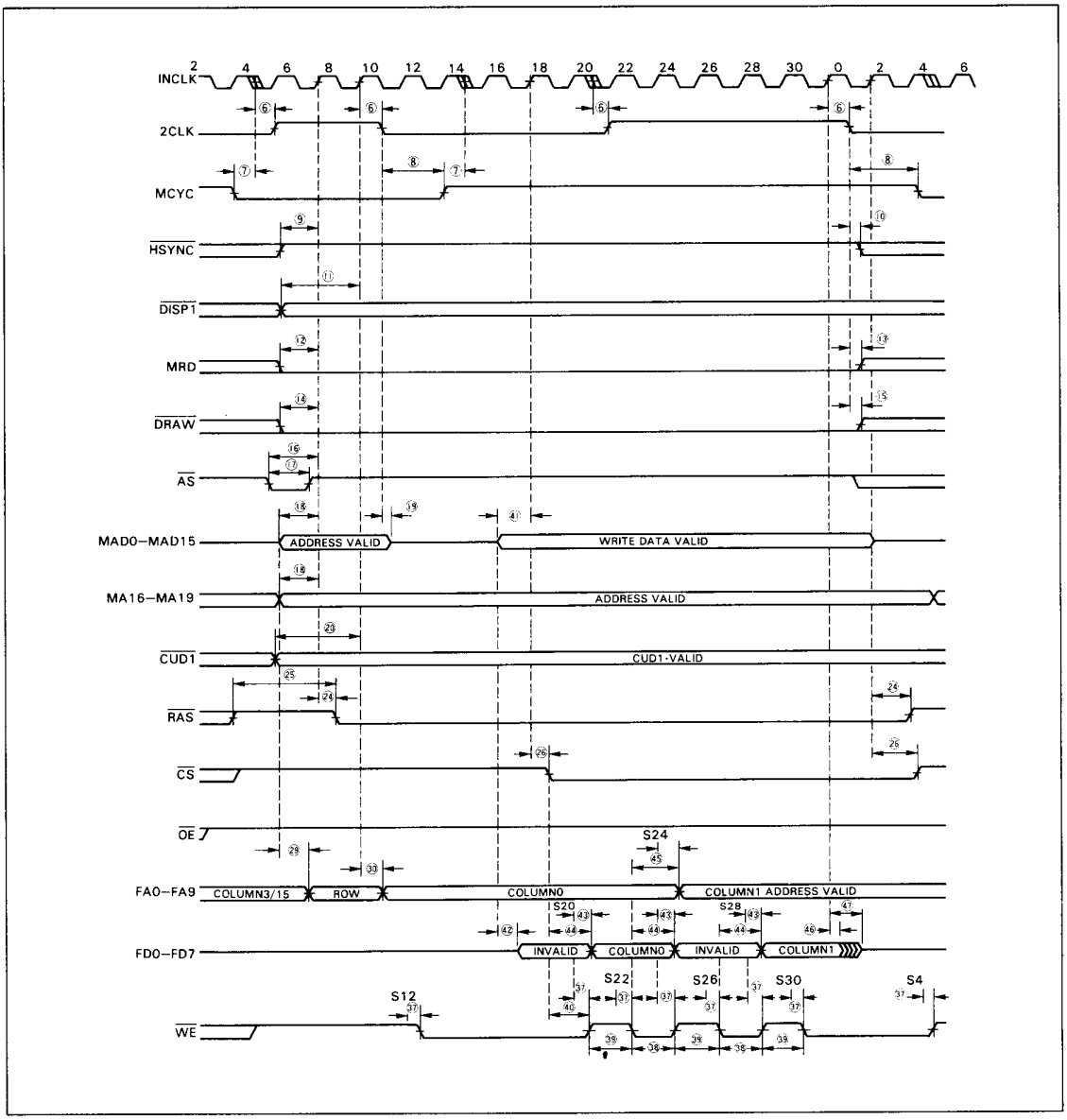


Figure 15 1MCYC Draw Write (2 Chips)

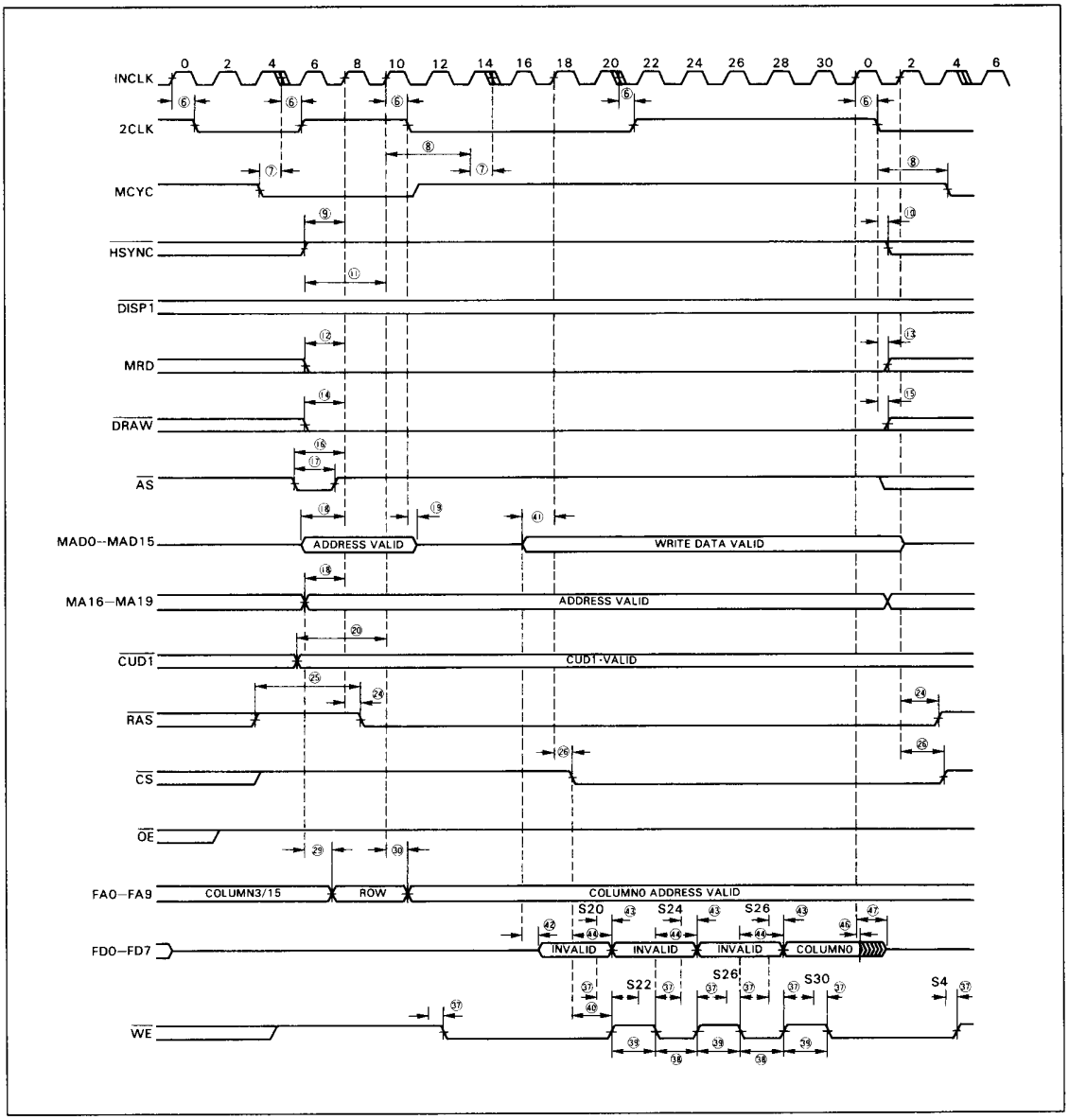


Figure 16 1MCYC Draw Write (4 Chips)

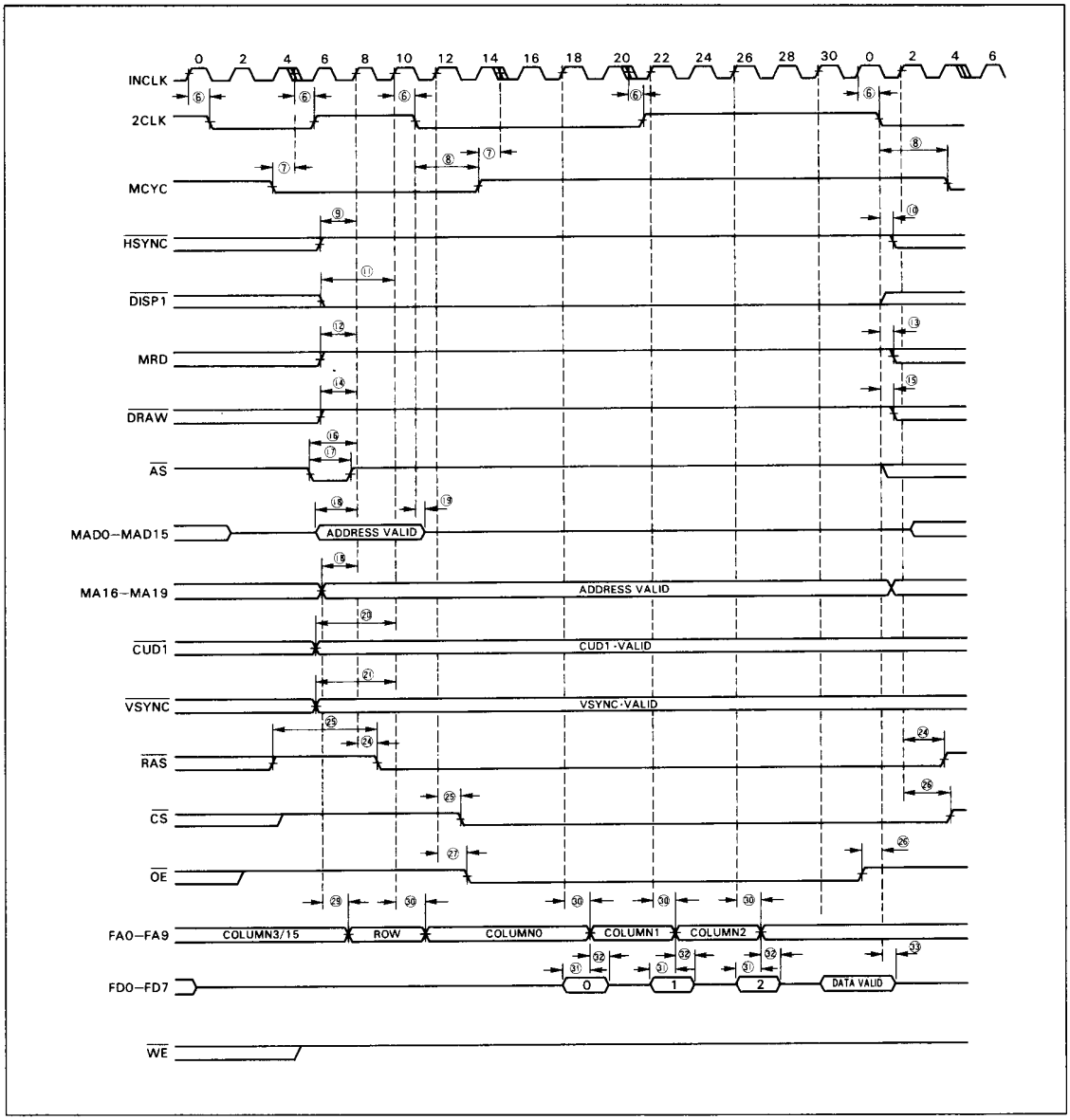


Figure 17 1MCYC Display Read (1 or 2 Chips)

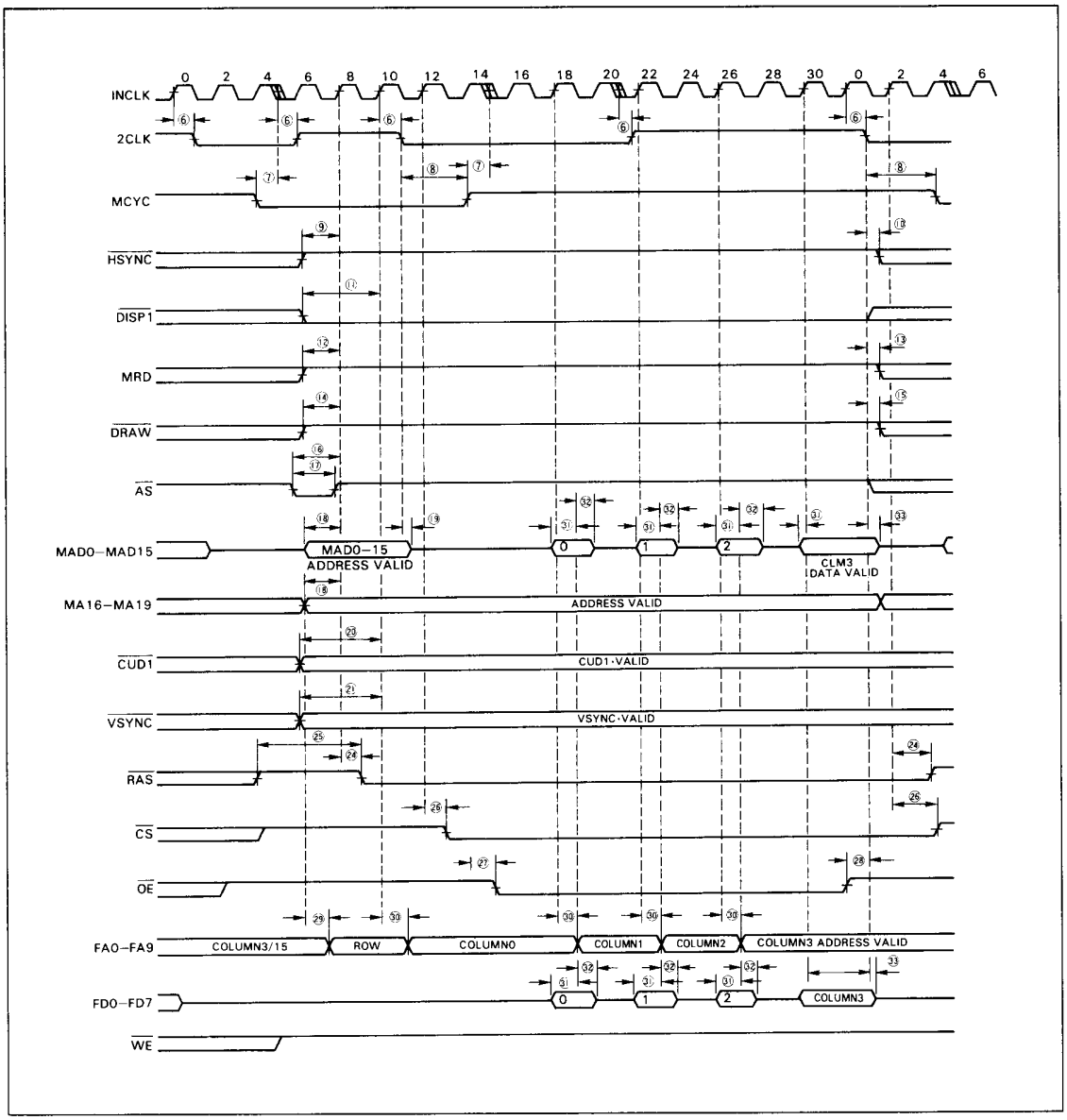


Figure 18 1MCYC Display Read (4 Chips)

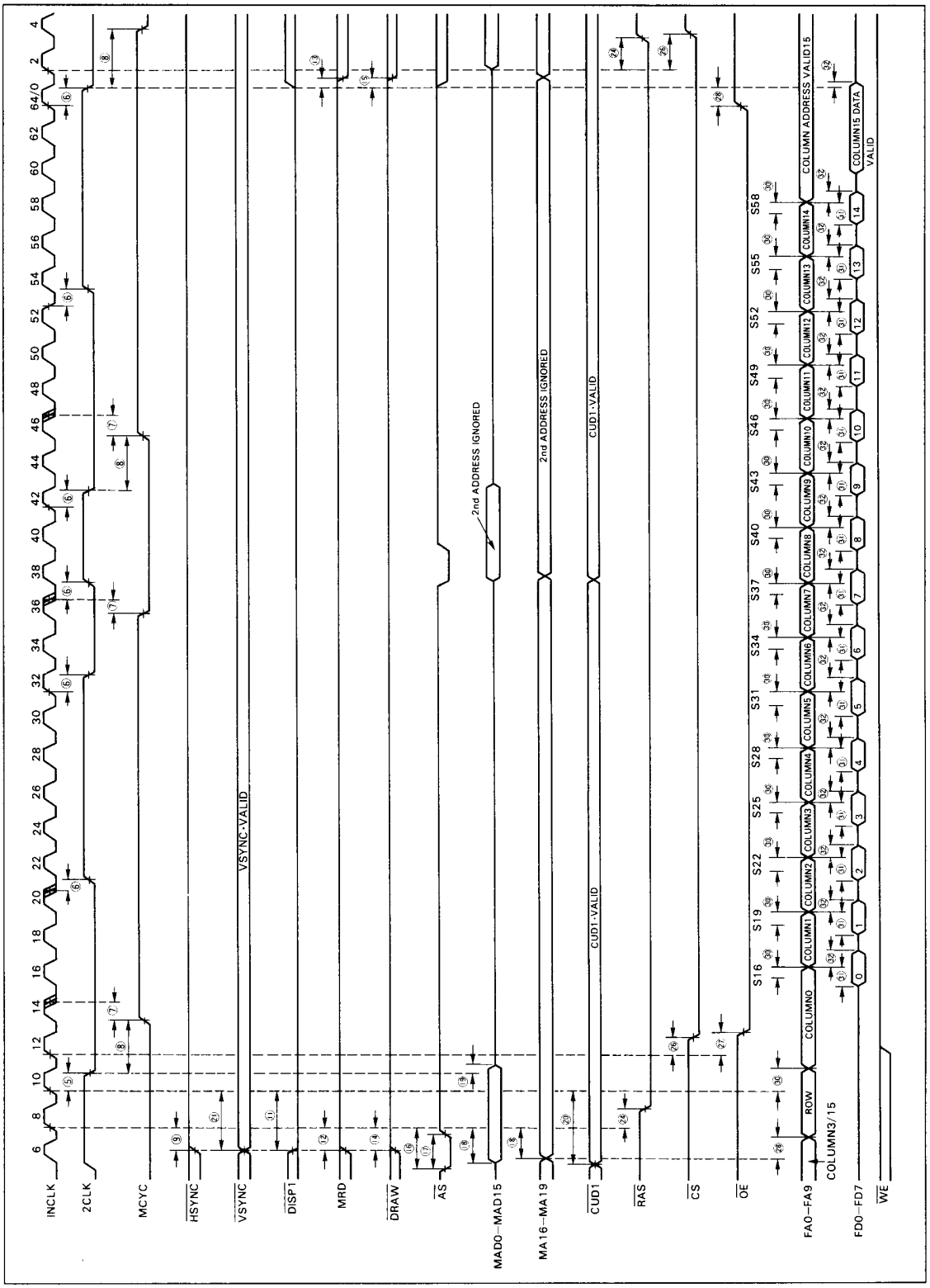


Figure 19 1MCYC Display Read (1 or 2 Chips)

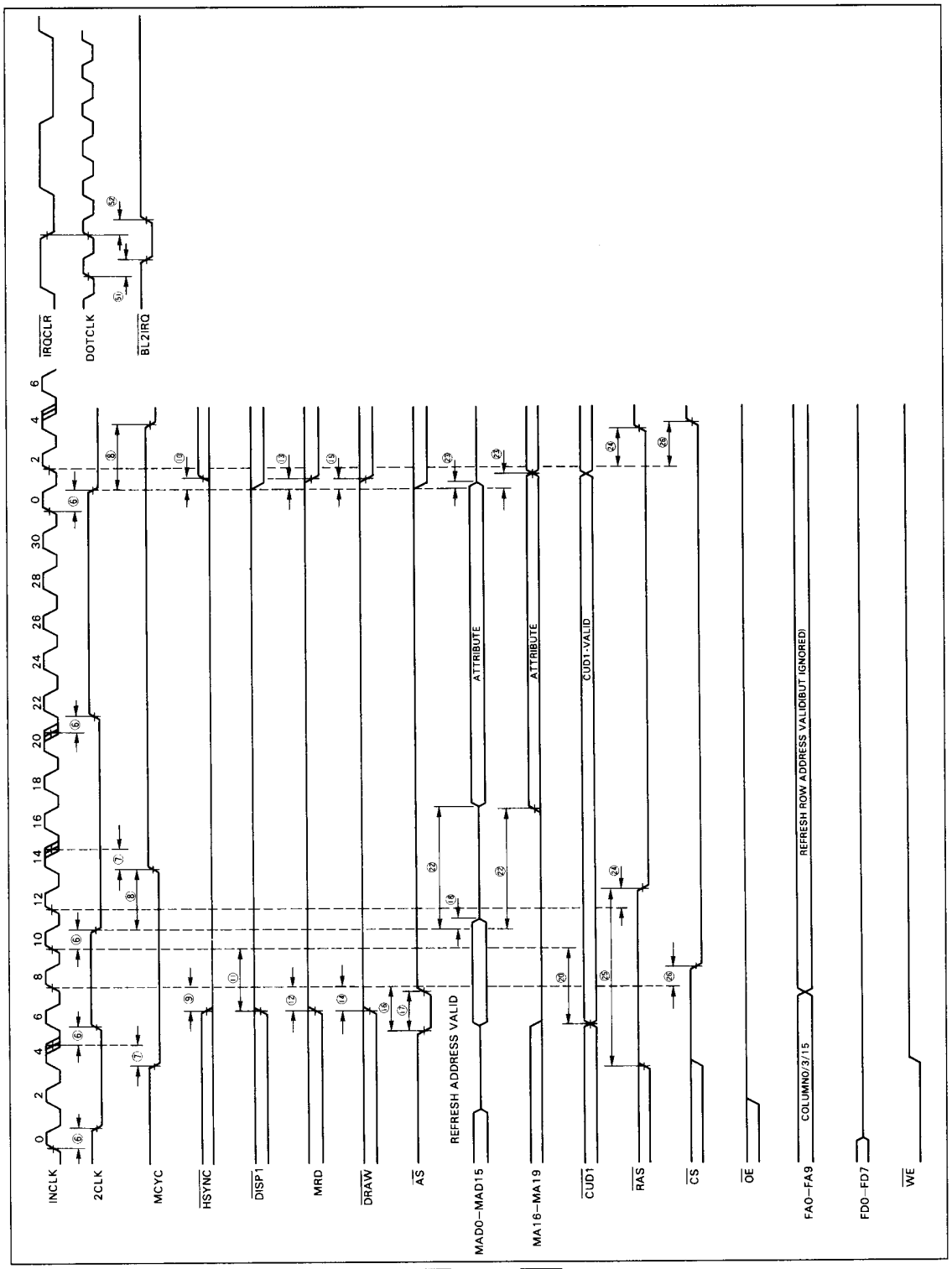
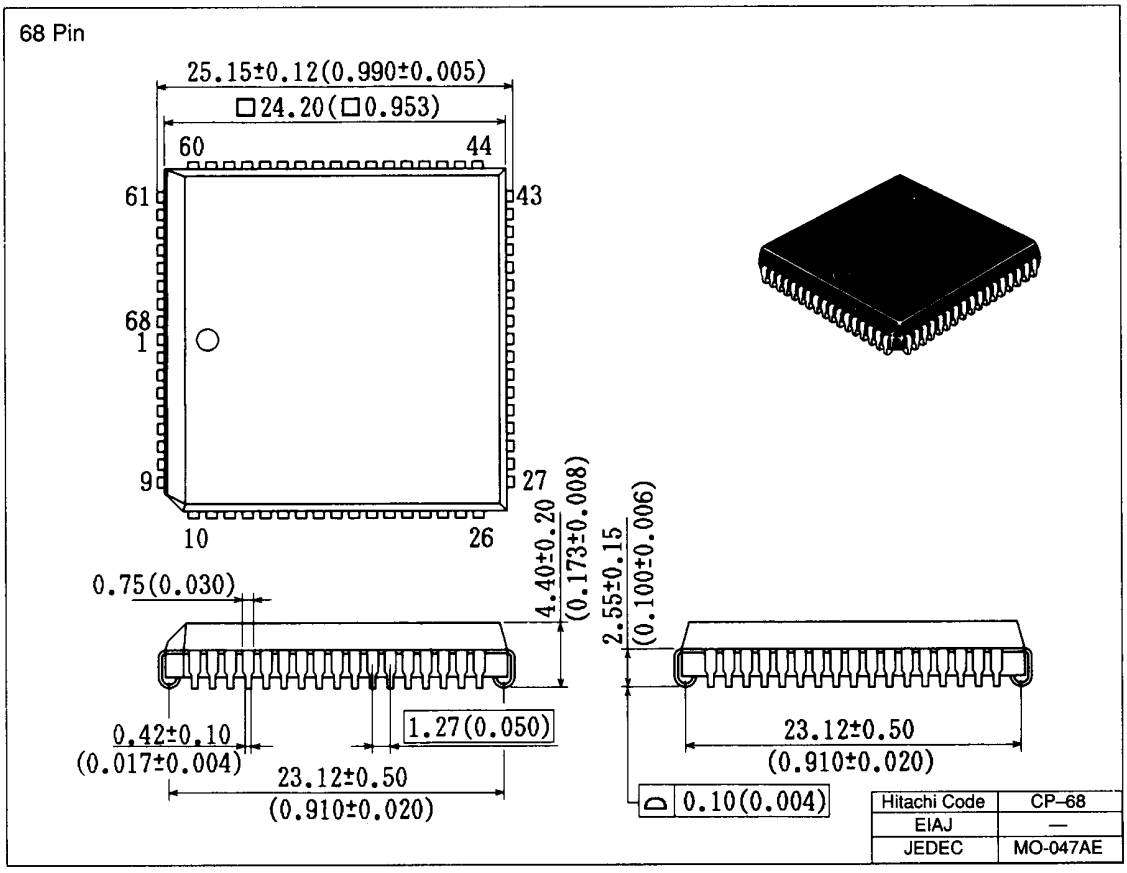


Figure 20 $\overline{CS}$ before $\overline{RAS}$ Refresh

Refer to application note (No. ADE-507-001) for detail of this product.

Package Dimensions

Unit: mm (inch)



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